IN THE CLAIMS:

1. (Currently Amended): A method for managing a read request, comprising:

receiving, at a first storage controller, a read request for a data block;

allocating a memory buffer for the data block from a memory pool that includes a first memory on the first storage controller and a second memory on a second storage controller, wherein the memory buffer resides in the second memory;

retrieving the data block from a storage device; and

caching the data block in the memory buffer.

2. (Currently Amended): The method of claim 1, wherein the first storage controller includes a first switch and the second controller includes a second switch.

3. (Original): The method of claim 2, wherein the first switch and the second switch are coupled using a switch-to-switch path.

4. (Original): The method of claim 3, wherein the step of caching comprises storing the data block in the second memory via the switch-to-switch path.

5. (Currently Amended): The method of claim 3, wherein the step of retrieving the data block comprises retrieving the data block from the storage device using a drive adapter on the second storage controller via the switch-to-switch path.

6. (Currently Amended): The method of claim 2, wherein the step of retrieving the data block comprises retrieving the data block from the storage device using a drive adapter on the first storage controller via the first switch.

7. (Currently Amended): A method for managing a read request, comprising:

receiving, at a first storage controller, a read request for a data block; and

retrieving the data block from a memory pool that includes a first memory on the first <u>storage</u> controller and a second memory on a second <u>storage</u> controller, wherein the data block resides in the second memory.

8. (Currently Amended): The method of claim 7, wherein the first <u>storage</u> controller includes a first switch and the second <u>storage</u> controller includes a second switch.

9. (Original): The method of claim 8, wherein the first switch and the second switch are coupled using a switch-to-switch path.

10. (Original): The method of claim 9, wherein the step of retrieving the data block from the memory pool comprises retrieving the data block from the second memory using the switch-to-switch path.

11. (Currently Amended): A method for managing a write request, comprising:

receiving, at a first <u>storage</u> controller, a write request for a data block;

allocating a primary data buffer for the data block in a first memory and a mirror data buffer for the data block in a second memory, wherein the first memory resides on one of the first <u>storage</u> controller and a second <u>storage</u> controller and the second memory resides on the other of the first <u>storage</u> controller and the second <u>storage</u> controller;

storing write data for the data block in the primary data buffer; and

mirroring the write data in the mirror data buffer.

12. (Currently Amended): The method of claim 11, wherein the first <u>storage</u> controller includes a first switch and the second <u>storage</u> controller includes a second switch.

13. (Original): The method of claim 12, wherein the first switch and the second switch are coupled using a switch-to-switch path.

14. (Currently Amended): The method of claim 13, wherein the first memory resides on the second <u>storage</u> controller and the step of storing write data for the data block in the

primary data buffer comprises storing the write data in the primary data buffer via the switch-to-switch path.

15. (Currently Amended): The method of claim 13, wherein the second memory resides on the second storage controller and the step of mirroring the write data in the mirror data buffer comprises storing the write data in the mirror data buffer via the switch-to-switch path.

16. (Currently Amended): The method of claim 13, further comprising:

writing the write data to a storage device using a drive adapter on the second storage controller via the switch-to-switch path.

17. (Currently Amended): The method of claim 12, further comprising:

writing the write data to a storage device using a drive adapter on the first storage controller via the first switch.

18. (Currently Amended): An apparatus, in a first storage controller, comprising:

a host adapter that provides a connection to a host;

a processor;

a first memory controller that manages a connection to a memory;

a drive adapter that provides a connection to a storage device;

a first switch that connects the host adapter, the processor, (the first memory) controller, and the drive adapter; and

a switch-to-switch path that connects the first switch to a second switch on a second storage controller.

19. (Currently Amended): The apparatus of claim 18, wherein the host adapter receives a read request for a data block; and

wherein the processor allocates a memory buffer for the data block from a memory pool that includes [[a]] the first memory on the first storage controller and a second memory on the second storage controller, wherein the memory buffer resides in

the second memory; retrieves the data block from a storage device; and caches the data block in the memory buffer via the switch-to-switch path.

6
20. (Original): The apparatus of claim 19, wherein the processor retrieves the data block from the storage device using the drive adapter via the first switch.

5
21. (Currently Amended): The apparatus of claim 19, wherein the processor retrieves the data block from the storage device using a drive adapter on the second storage controller via the switch-to-switch path.

1/21
22. (Currently Amended): The apparatus of claim 18, wherein the host adapter receives a read request for a data block; and

A q

wherein the processor retrieves the data block from a memory pool that includes [[a]] the first memory on the first storage controller and a second memory on the second storage controller, wherein the data block resides in the second memory.

23. (Currently Amended): The apparatus of claim 18, wherein the host adapter receives a write request for a data block; and

wherein the processor allocates a primary data buffer for the data block in a first memory and a mirror data buffer for the data block in a second memory, wherein the first memory primary data buffer resides on one of the first storage controller and the second storage controller and the second memory mirror data buffer resides on the other of the first storage controller and the second storage controller; wherein the processor stores write data for the data block in the primary data buffer; and wherein the processor mirrors the write data in the mirror data buffer.

24. (Currently Amended): The apparatus of claim 23, wherein the first memory primary data buffer resides on the second storage controller and the processor stores the write data in the primary data buffer via the switch-to-switch path.

25. (Currently Amended): The apparatus of claim 23, wherein the ~~second memory~~ <u>mirror data buffer</u> resides on the second <u>storage</u> controller and the processor stores the write data in the mirror data buffer via the switch-to-switch path.

26. (Original): The apparatus of claim 23, wherein the processor writes the write data to a storage device using the drive adapter via the first switch.

27. (Currently Amended): The apparatus of claim 23, wherein the processor writes the write data to a storage device using a drive adapter on the second <u>storage</u> controller via the switch-to-switch path.